IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A method of fabricating a transistor on a substrate, the method comprising:

forming a first source/drain region on the substrate;

vertically forming a body region on the first source/drain region as a fully depleted structure, wherein vertically forming the body region includes vertically growing an epitaxial layer such that the body region is formed having a width that is sufficiently thin relative to a doping concentration (NA) of the body region such that a bulk charge (QB) is negligible in transistor operation, and wherein the body region includes opposing sidewall surfaces;

forming a second source/drain region on the body region;

forming a first gate on a first one of the opposing sidewall surfaces separated from the first one of the opposing sidewall surfaces by a first oxide layer and

forming a second gate on a second one of the opposing sidewall surfaces separated from the second one of the opposing sidewall surfaces by a second oxide layer.

2. (Original) The method of claim 1, wherein fabricating a transistor includes fabricating the transistor on a p-type bulk silicon substrate.

3. (Previously Presented) The method of claim 1, wherein forming the body region includes forming the body region having a thickness of less than 0.2 microns.

4. (Previously Presented) The method of claim 1, wherein forming the transistor includes forming the body region having a thickness of about 0.4 microns.

5. (Original) The method of claim 1, wherein forming the first source/drain region includes forming the first source/drain region using ion implantation.

6. (Original) The method of claim 1, wherein forming the first source/drain region includes vertically growing an epitaxial layer.

7. (Original) The method of claim 1, wherein forming the first source/drain region includes using ion implantation and includes vertically growing an epitaxial layer.

8. (Previously Presented) A method of fabricating a transistor on a substrate, the method comprising:

forming a first source/drain region on the substrate;

vertically forming a body region on the first source/drain region, wherein vertically forming the body region includes vertically growing an epitaxial layer such that the body region is formed as a single crystalline structure having a width that is sufficiently thin relative to a doping concentration (NA) of the body region such that a bulk charge (QB) is negligible in transistor operation, and wherein the body region includes opposing sidewall surfaces;

forming a second source/drain region on the body region;

forming a first gate on a first one of the opposing sidewall surfaces separated from the first one of the opposing sidewall surfaces by a first oxide layer; and

forming a second gate on a second one of the opposing sidewall surfaces separated from the second one of the opposing sidewall surfaces by a second oxide layer, wherein the body region, the first gate, and the second gate are formed such that biasing the first and the second gates fully depletes the body region.

9. (Previously Presented) A method of fabricating a transistor on a substrate, the method comprising:

forming a first conductivity type first source/drain region on the substrate;

vertically forming a second conductivity type body region on the first source/drain layer, wherein vertically forming the body region includes vertically growing an epitaxial layer as a fully depleted structure such that the body region is formed as a single crystalline structure having a width that is sufficiently thin relative to a doping concentration (NA) of the body region

such that a bulk charge (QB) is negligible in transistor operation, and wherein the body region includes opposing sidewall surfaces;

forming a first conductivity type second source/drain region on the body region layer;

forming a first gate on a first one of the opposing sidewall surfaces separated from the first one of the opposing sidewall surfaces by a first oxide layer; and

forming a second gate on a second one of the opposing sidewall surfaces separated from the second one of the opposing sidewall surfaces by a second oxide layer.

10. (Original) The method of claim 9, wherein forming a first conductivity type first source/drain region includes vertically growing a p-type epitaxial layer.

11. (Original) The method of claim 9, wherein forming a first conductivity type first source/drain region includes vertically growing an n-type epitaxial layer.

12. (Previously Presented) The method of claim 9, wherein vertically forming a second conductivity type body region includes forming, wherein forming the second conductivity type body region having a thickness of less than 0.2 microns.

13. (Previously Presented) A method of fabricating a transistor on a substrate, the method comprising:

vertically growing an n-type epitaxial first source/drain region on the substrate;

vertically forming a second conductivity type body region on the first source/drain layer as a fully depleted structure, wherein vertically forming the body region includes vertically growing an epitaxial layer such that the body region is formed as a single crystalline structure having a width that is sufficiently thin relative to a doping concentration (NA) of the body region such that a bulk charge (QB) is negligible in transistor operation, and wherein the body region includes opposing sidewall surfaces;

vertically growing an n-type epitaxial second source/drain region on the body region layer;

forming a first gate on a first one of the opposing sidewall surfaces separated from the first one of the opposing sidewall surfaces by a first oxide layer; and

forming a second gate on a second one of the opposing sidewall surfaces separated from the second one of the opposing sidewall surfaces by a second oxide layer.

14. (Previously Presented) A method of fabricating a transistor on a substrate, the method comprising:

vertically forming a body region extending outwardly from the substrate, wherein vertically forming the body region includes forming the body region as a fully depleted structure such that the body region is formed as a single crystalline structure having a width that is sufficiently thin relative to a doping concentration (NA) of the body region such that a bulk charge (QB) is negligible in transistor operation, and wherein vertically forming the body region includes forming the body region with opposing sidewall surfaces;

forming a first source/drain region adjacent to the body region;

forming a second source/drain region adjacent to the body region;

forming a first gate on a first one of the opposing sidewall surfaces separated from the first one of the opposing sidewall surfaces by a first oxide layer; and

forming a second gate on a second one of the opposing sidewall surfaces separated from the second one of the opposing sidewall surfaces by a second oxide layer.

15. (Original) The method of claim 14, wherein fabricating a transistor on a substrate includes fabricating the transistor on an insulator layer.

16. (Original) The method of claim 14, wherein forming a first source/drain region adjacent to the body region includes encasing a portion of the body region with Arsenic silicate glass (ASG) and annealing the ASG.

17. (Original) The method of claim 16, wherein encasing a portion of the body region with Arsenic silicate glass (ASG) includes depositing the ASG using chemical vapor deposition (CVD).

18. (Original) The method of claim 14, wherein forming a first source/drain region adjacent to the body region includes encasing a portion of the body region with Borosilicate silicate glass (BSG) and includes annealing the BSG.

19. (Original) The method of claim 18, wherein encasing a portion of the body region with Borosilicate silicate glass (BSG) includes depositing the BSG using chemical vapor deposition (CVD).

20. (Previously Presented) A method of fabricating a transistor on a substrate, the method comprising:

vertically forming a body region extending outwardly from the substrate, including forming the body region as a fully depleted structure such that the body region is formed as a single crystalline structure having a width that is sufficiently thin relative to a doping concentration (NA) of the body region such that a bulk charge (QB) is negligible in transistor operation, and wherein vertically forming the body region includes forming the body region with opposing sidewall surfaces;

forming a first source/drain region adjacent to the body region, wherein forming the first source/drain region adjacent to the body region includes encasing a portion of the body region with Arsenic silicate glass (ASG) and annealing the ASG;

forming a second source/drain region adjacent to the body region, wherein forming the second source/drain region adjacent to the body region includes encasing a portion of the body region with Arsenic silicate glass (ASG) and annealing the ASG;

forming a first gate on a first one of the opposing sidewall surfaces separated from the first one of the opposing sidewall surfaces by a first oxide layer; and

forming a second gate on a second one of the opposing sidewall surfaces separated from the second one of the opposing sidewall surfaces by a second oxide layer.

21. (Previously Presented) A method of forming a dual-gated transistor on a substrate, comprising:

forming a first source/drain region on the substrate;

vertically forming a body region with a fully depleted structure on the first source/drain region, including vertically growing an epitaxial layer such that the body region is formed as a single crystalline structure having a width that is sufficiently thin relative to a doping concentration (NA) of the body region such that a bulk charge (QB) is negligible in transistor operation;

forming a second source/drain region on the body region;

forming a first gate on a first one of opposing sidewall surfaces of the body region separated from the first one of the opposing sidewall surfaces by a first oxide layer; and

forming a second gate on a second one of the opposing sidewall surfaces separated from the second one of the opposing sidewall surfaces by a second oxide layer, such that a threshold voltage for the transistor depends only on a thickness of the first and second oxides and the width of the body region.

22. (Previously Presented) The method of claim 21, including fabricating the dual-gated transistor on a p-type bulk silicon substrate.

23. (Previously Presented) The method of claim 21, including forming the body region, the first gate, and the second gate such that biasing the first and the second gates fully depletes the body region.

24. (Previously Presented) The method of claim 21, including forming the first source/drain region using ion implantation.

25. (Previously Presented) The method of claim 21, wherein forming the first source/drain region includes vertically growing an epitaxial layer.

26. (Previously Presented) The method of claim 21, wherein forming the first source/drain region includes using ion implantation and includes vertically growing an epitaxial layer.

27. (Previously Presented) The method of claim 21, including encasing a portion of the body region with Arsenic silicate glass (ASG) and annealing the ASG.

28. (Previously Presented) The method of claim 27, including performing chemical vapor deposition (CVD) to deposit the ASG.

29. (Previously Presented) The method of claim 21, wherein forming a first source/drain region adjacent to the body region includes encasing a portion of the body region with Borosilicate silicate glass (BSG) and includes annealing the BSG.

30. (Previously Presented) The method of claim 29, including using chemical vapor deposition (CVD) to deposit the BSG.

31. (Previously Presented) The method of claim 1, wherein the method further includes forming an insulating layer between the body region and the substrate.

32. (Previously Presented) The method of claim 8, wherein the method further includes forming an insulating layer between the body region and the substrate.

33. (Previously Presented) The method of claim 9, wherein the method further includes forming an insulating layer between the body region and the substrate.

34. (Previously Presented) The method of claim 13, wherein the method further includes forming an insulating layer between the body region and the substrate.

35. (Previously Presented) The method of claim 20, wherein the method further includes forming an insulating layer between the body region and the substrate.

36. (Previously Presented) The method of claim 21, wherein the method further includes forming an insulating layer between the body region and the substrate.

37. (New) The method of claim 1, wherein forming a body region includes forming the body region such that the body region is not formed across other surfaces.

38. (New) The method of claim 1, wherein forming the body region having a width that is sufficiently thin relative to a doping concentration (NA) of the body region includes forming the body region with a width and doping such that a threshold voltage is insensitive to fluctuations in the doping concentration.